13.3 A Monolithic Low-Bandwidth Jitter-Cleaning PLL with Hitless Switching for SONET/SDH Clock Generation

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In SONET/SDH systems, transmit timing-reference-clock signals are often transported through the backplane to line cards. To guarantee system reliability, redundant reference clocks are commonly required and a switch module is used to toggle among them as needed. To avoid downstream system interruption, switching between 2 reference clock signals, with arbitrary relative phase, shall not cause short-term phase transients, or so-called phase hits. Stringent jitter performance is also required of these clock signals. However, signal loss and noise coupling along the clock distribution path may degrade the clock signal received at the line card by contributing wideband jitter noise. Thus, it is usually necessary to use a low-bandwidth PLL to attenuate the jitter before using the received clock for a line card transmitter. Typical designs for reference clock modules include a multiplexer followed by a discrete low bandwidth PLL (including a high-quality VCXO) and a clock multiplier unit (CMU), as shown in Fig. 13.3.1. This discrete approach is not only bulky and costly, but it also suffers from analog issues such as noise coupling and high power dissipation.; The proposed system addresses these issues by incorporating a low-bandwidth (e.g. as low as 800Hz) DSP-based PLL with a high-performance VCO and a hitless switching feature into a single chip. The digital hitless switching technique and the low-noise VCO control circuits are discussed in the following paragraphs.

Figure 13.3.1 shows a typical transient response of a Type-II PLL during the reference switching with phase offsets. The transient is the response of the PLL to the changing PFD output. The digital implementation of the proposed "hitless" switching technique is shown in Fig. 13.3.2. In each reference path, the charge pump (CP) output is digitized by a 311MHz 1b ΔΣ ADC modulator, whose output is decimated and selectively fed into the digital loop filter (DLF). If CLK A is driving the PLL, SWA is opened, and the loop drives $\Delta\phi_{PFDA}$ to 0 since DECA is muxed into the DLF. Meanwhile, SWB closes to pass DECB to the autozero (AZ) loop. The AZ loop contains an accumulator and a 6b current DAC. The digitized phase error from the CLK B path is filtered by the accumulator and the result drives the offset DAC, injecting a DC current at the modulator summing node. Since the accumulator extracts the DC component of the decimator output (equal to $\Delta\phi_{PFDB}$), the AZ loop drives DECB to zero. At switching, the multiplexer passes DECB instead of DECA to the DLF, with SWB opened, SWA closed, and DAC_B frozen. Since both digital PFD path outputs are driven toward zero and the PLL bandwidth is low, the PLL output phase switching transients are minimized. Figure 13.3.3 shows a typical switching phase transient with the loop bandwidth set to 6.4kHz. The maximum steady-state phase error is well below 200ps (2 DAC LSBs). Both the maximum phase step and slopes are within MTIE specifications [1].

When CLK A and B have a small frequency offset, the accumulated phase error will eventually saturate the PFD ΔΣ ADC in the AZ loop of the unselected input clock. Figure 13.3.2 shows a pulse swallow control block added to address this issue: $\Delta\phi_{PFDB}$ is monitored by a 16×-oversampling edge detector. When $\Delta\phi_{PFDB}$ reaches one 311MHz clock period (T_{clk311}), a one-shot ÷15 or ÷17 is triggered in the ÷16 feedback divider, so that the feedback clock edge is advanced or delayed by T_{clk311}. Meanwhile, a corresponding offset is added to the offset DAC control word so that the net decimator output remains zero. The offset DAC is designed to provide $\pm 2T_{clk311}$ phase range to avoid overflow.

Since VCO noise is suppressed by the PLL only at frequencies below the closed-loop bandwidth, the noise performance of the low-bandwidth PLL is greatly dictated by the VCO phase noise. Additionally, although the VCO gain K_{vco} should be made low to minimize front-end noise contribution, high K_{vco} may be required from the demanded VCO tuning range. To resolve these opposing requirements, we partitioned the varactor into multiple sub-varactors to reduce the individual K_{vco} but preserve the desired tuning range [2]. The proposed design includes an LC-oscillator with 128 digitally-controlled sub-varactors. As shown in Fig. 13.3.4, a digital loop filter is used to avoid the noise coupling susceptibility of traditional analog loop filters [3]. The gain factors for the digital feedforward and accumulator paths are programmable to provide the desired closed-loop bandwidth and zero frequency. Figure 13.3.4 shows the relative bit locations for the feedforward path (F) and integration path (I) in the 46b control word of DLF at different bandwidth settings. These 46 bits are then ΔΣ-modulated down to 20 bits and converted into analog voltages via multiple 2nd-order ΔΣ DACs driving sub-varactors. Instead of using 128 DACs that would have consumed significant chip area and power, 8 barrel-shifted DACs are driven by the 20b output of the DLF, with an offset equal to 25% of DAC full-scale added between neighboring DACs. The 20b output of the DLF is decoded by a digital DAC expander to direct where the 8 DAC outputs are connected among the 128 sub-varactors via 128 multiplexers. Therefore, at any given time, no more than 8 sub-varactors are actively driven by the feedforward path while the rest are tied to either supply or ground. Due to the 25% offset between the DACs, Fig. 13.3.5 shows that the boundary 4 DACs are always at rail/ground while the middle ones overlap to mitigate the nonlinear C-V transfer curve of each sub-varactor. When the DAC bank needs to move to a new location, a boundary DAC is barrel-shifted to the other side of the bank, from rail to ground (or vise versa) before it enters the analog tuning mode again. With a varactor tuning range of 75MHz, the effective K_{vco} for DAC noise is 75MHz/(128×0.25)/2V<1.2MHz/V, where 2V is the DAC output full scale and 0.25 is the digital offset between each DAC. This implementation greatly relaxes the noise requirement for the PFD ADC, the varactor DACs, and the digital loop filter. The low-noise LC VCO includes a finger capacitor array, a cross-coupled CMOS amplifier, and a high-Q package inductor. The overall LC tank quality factor is estimated to be 30.

Figure 13.3.6 shows a phase noise measurement of the chip output clock at 622.08MHz, and the performance summary when the PLL loop bandwidth is set to 800Hz. Fabricated in a 0.25μm CMOS process, the 3.2×5.1mm² die is packaged in an 11×11mm² ceramic BGA. The power consumption is 350mW from a 3.3V supply when providing a single clock output. Jitter generation in the OC-48 band is 0.8ps and is 0.4ps in OC-192 band, well suited for OC-192 (10Gb/s) SONET/SDH systems.

References:

[1] Telcordia Technologies, "Output Signal Criteria," chap. 5*, GR-1244-Core,* Dec., 2000.

[2] T-H Lin and W. J. Kaiser, "A 900-MHz 2.5-mA CMOS Frequency Synthesizer with an Automatic SC Tuning Loop," *IEEE J. Solid-State Circuits*, vol. 36, pp. 424-431, Mar., 2001.

[3] M. H. Perrott, et al., "Digitally-Synthesized Loop Filter Circuit Particularly Useful for a Phase Locked Loop," *United States Patent 6,765,445*.

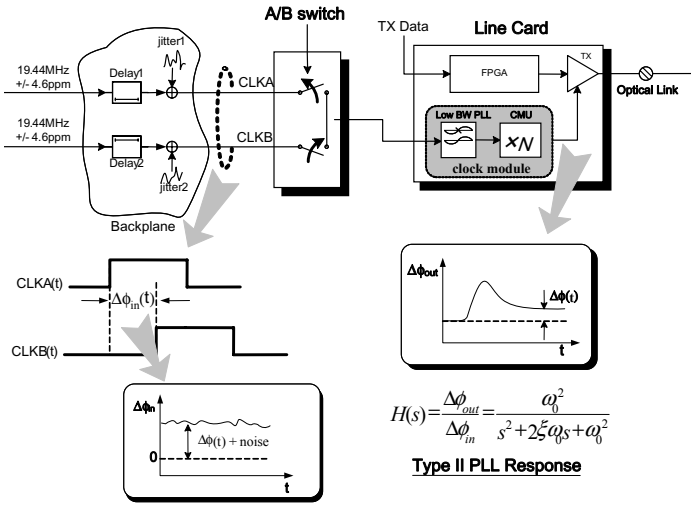


Figure 13.3.1: Phase transient incurred by reference-switching in SONET/SDH systems.

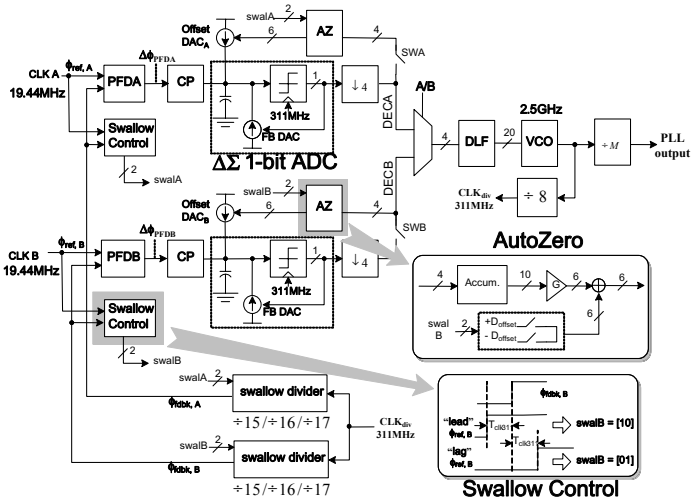


Figure 13.3.2: Digital implementation of hitless switching.

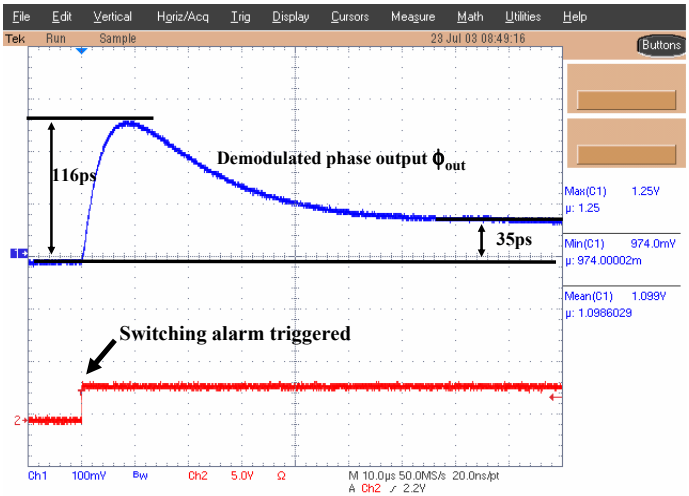


Figure 13.3.3: Output phase transient during A → B switching (loss of clock A) clock A and B are both 19.44MHz, with 180° phase difference.

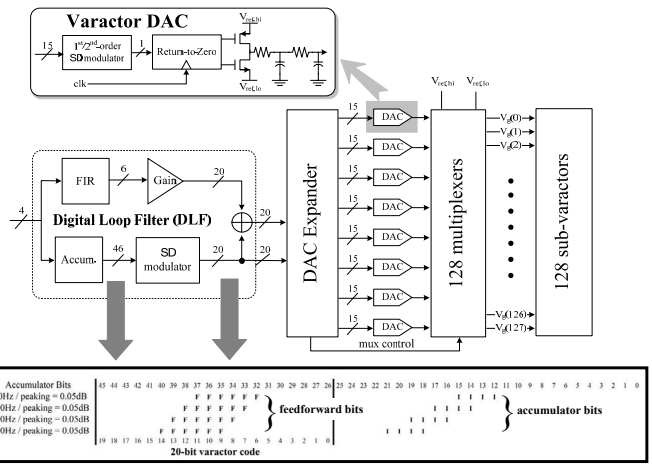


Figure 13.3.4: Digital loop filter (DLF) and VCO varactor control.

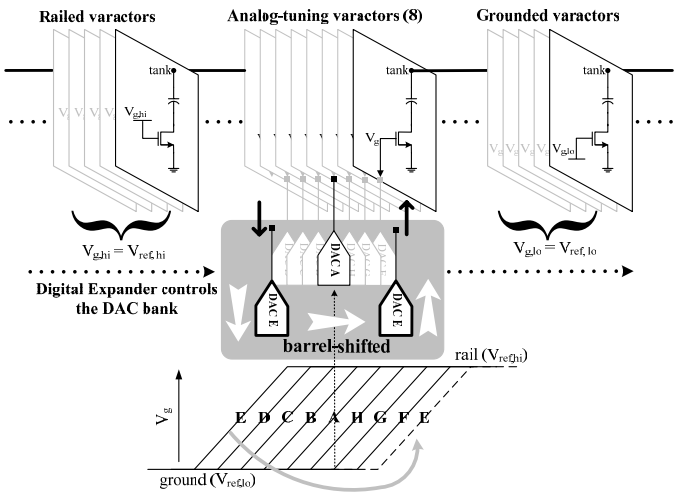
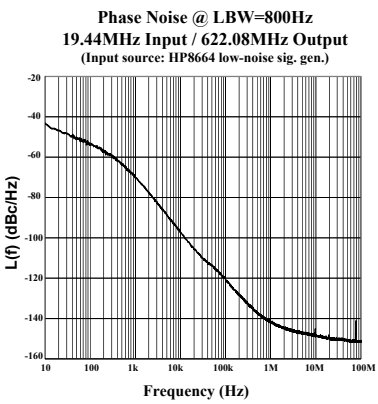


Figure 13.3.5: Barrel-shifted DACs move across sub-varactors.



Performance Summary

Technology	0.25µm-CMOS
Chip Area	3.2mm by 5.1mm
Package	11 X 11 CBGA
Power @ Vdd=3.3V	350mW
PLL Bandwidth (LBW)	800Hz, 1600Hz, 3200Hz, 6400Hz
During Reference Switch @ BW=800Hz	
Maximum Output Phase Step	200ps
Maximum Output Phase Slope	4.5 ns/ms
Jitter Generation @ BW=800Hz	
OC-48 (12kHz ~ 20MHz)	0.8ps
OC-192 (50kHz ~ 80MHz)	0.4ps

Figure 13.3.6: Output phase-noise measurement (622.08MHz) and performance summary.

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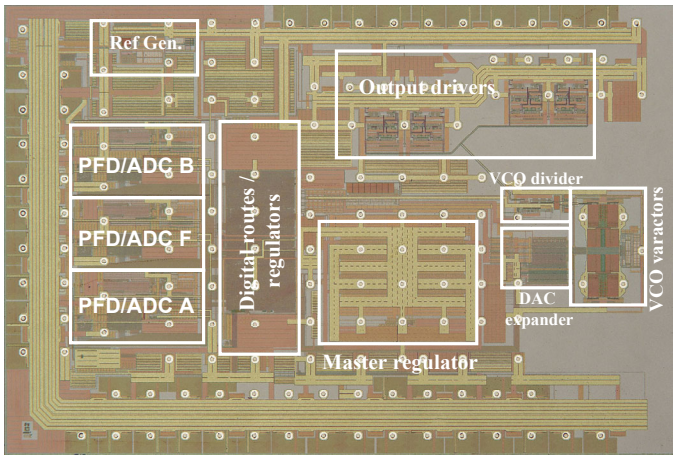

13.3.7: Die micrograph.

